

**HIGH CURRENT PHASE CONTROL
THYRISTOR INSULATED MODULE**

AZT805

Repetitive voltage up to **1800 V**
Mean forward current **819 A**
Surge current **30 kA**

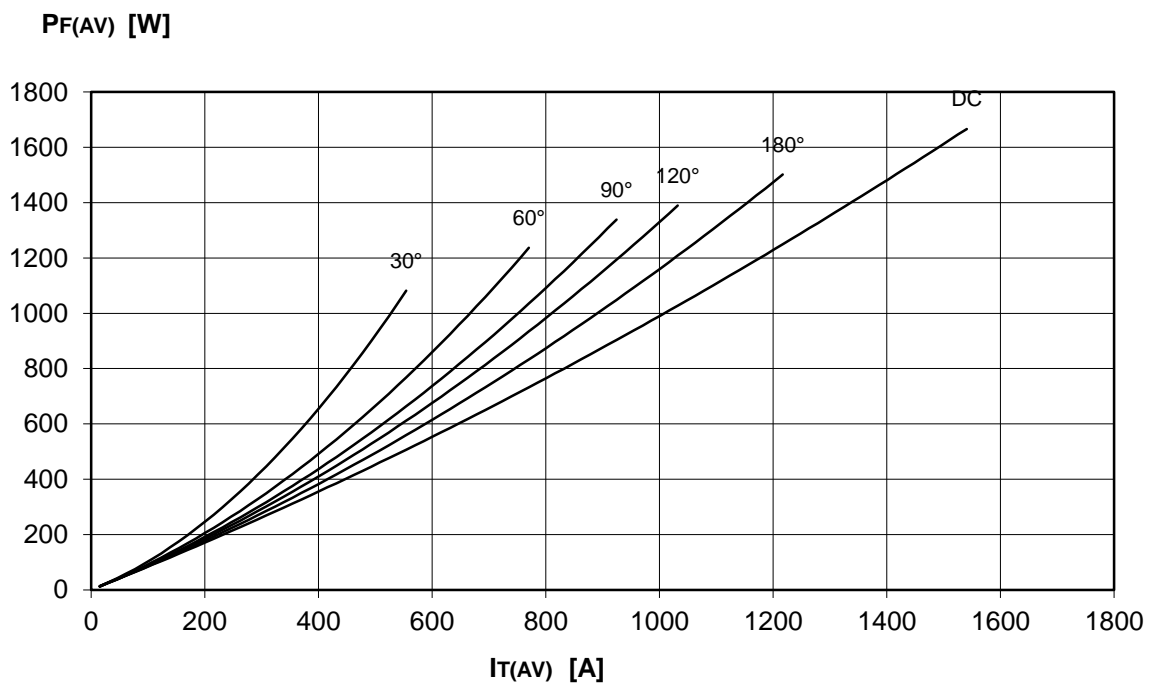
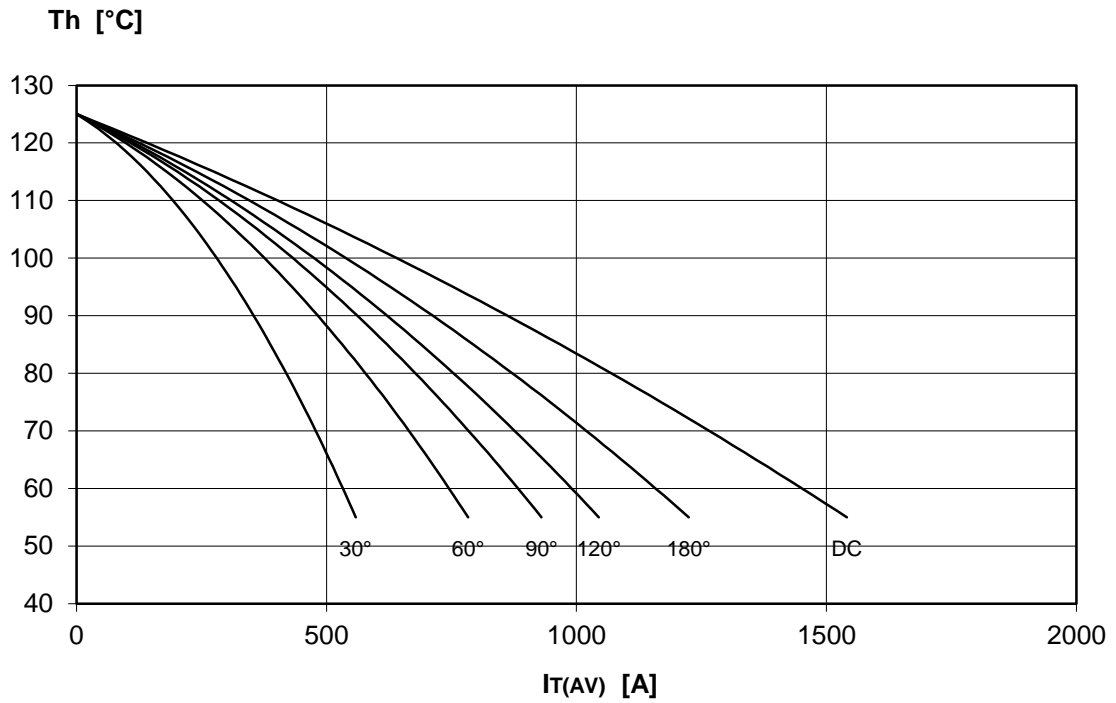
FINAL SPECIFICATION

Oct. 18 - Issue: 0

Symbol	Characteristic	Conditions	T _j [°C]	Value	Unit
BLOCKING					
V _{RRM}	Repetitive peak reverse voltage		125	1800	V
V _{RSM}	Non-repetitive peak reverse voltage		125	1900	V
V _{DRM}	Repetitive peak off-state voltage		125	1800	V
I _{RRM}	Repetitive peak reverse current		125	70	mA
I _{DRM}	Repetitive peak off-state current		125	70	mA
CONDUCTING					
I _{T(AV)}	Mean forward current	180° sin, 50 Hz, T _c =55°C, double side cooled		1243	A
I _{T(AV)}	Mean forward current	180° sin, 50 Hz, T _c =85°C, double side cooled		819	A
I _{TSM}	Surge forward current	Sine wave, 10 ms	125	30	kA
I ² t	I ² t	without reverse voltage		4500 x 10 ³	A ² s
V _T	On-state voltage	On-state current = 3000 A	25	1,51	V
V _{T(TO)}	Threshold voltage		125	0,82	V
r _T	On-state slope resistance		125	0,170	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% V _{DRM} up to 1050 A; gate 10V, 5Ω	125	200	A/μs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of V _{DRM}	125	1000	V/μs
t _d	Gate controlled delay time, typical	VD=100V; gate source 25V, 10Ω, tr=.5 μs	25	4	μs
t _q	Circuit commutated turn-off time, typical	dv/dt = 20 V/μs linear up to 75% V _{DRM}		350	μs
Q _{rr}	Reverse recovery charge	di/dt = -20 A/μs, I = 700 A	125		μC
I _{rr}	Peak reverse recovery current	VR= 50 V			A
I _H	Holding current, typical	VD=5V, gate open circuit	25	500	mA
I _L	Latching current, typical	VD=5V, tp=30μs	25	2500	mA
GATE					
V _{GT}	Gate trigger voltage	VD=5V	25	2,00	V
I _{GT}	Gate trigger current	VD=5V	25	250	mA
V _{GD}	Non-trigger gate voltage, min.	VD=V _{DRM}	125	0,25	V
V _{FGM}	Peak gate voltage (forward)			30	V
I _{FGM}	Peak gate current			10	A
V _{RGM}	Peak gate voltage (reverse)			5	V
P _{GM}	Peak gate power dissipation	Pulse width 100 μs		150	W
P _G	Average gate power dissipation			2	W
MOUNTING					
R _{th(j-c)}	Thermal impedance, DC	Junction to case, per element		42,0	°C/kW
R _{th(c-h)}	Thermal impedance	Case to heatsink, per element		20	°C/kW
T _j	Operating junction temperature			-30 / 125	°C
V _{ins}	RMS insulation voltage	50 hz, circuit to base, all terminal shorted	25	3000	V
T	Mounting torque	Case to heatsink		4,0 / 6,0	kN
		Busbars to terminals		12,0 / 18,0	kN
	Mass			1950	g
ORDERING INFORMATION : AZT805 S 18					
standard specification <input type="checkbox"/> <input type="checkbox"/> VRRM/100					

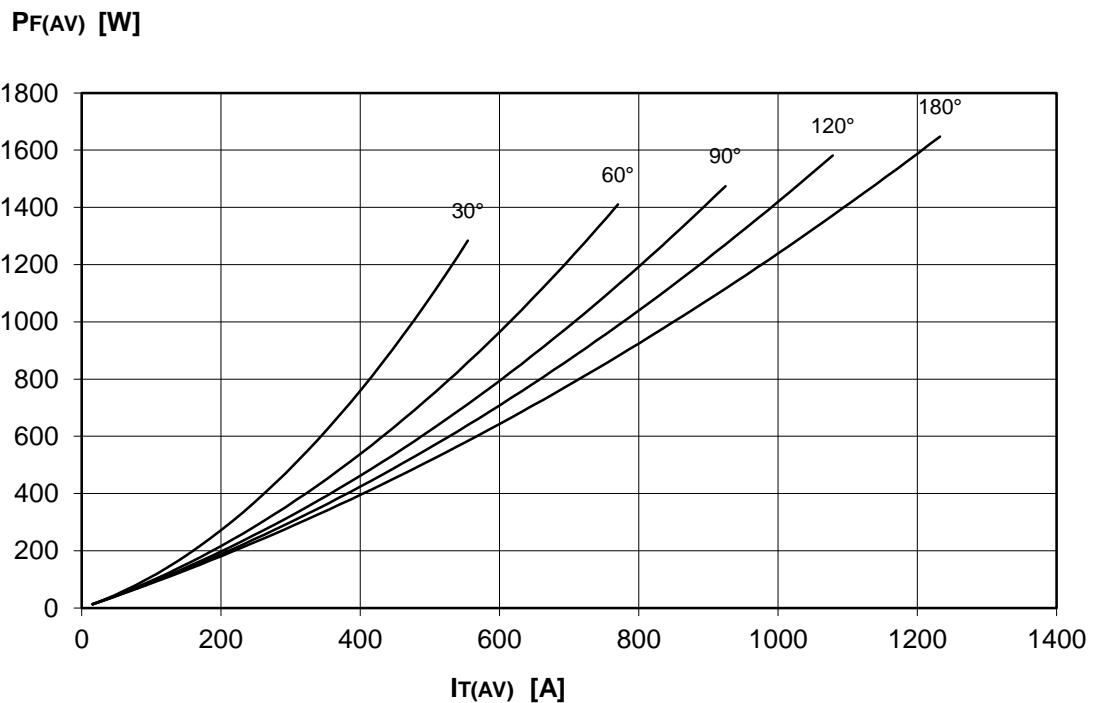
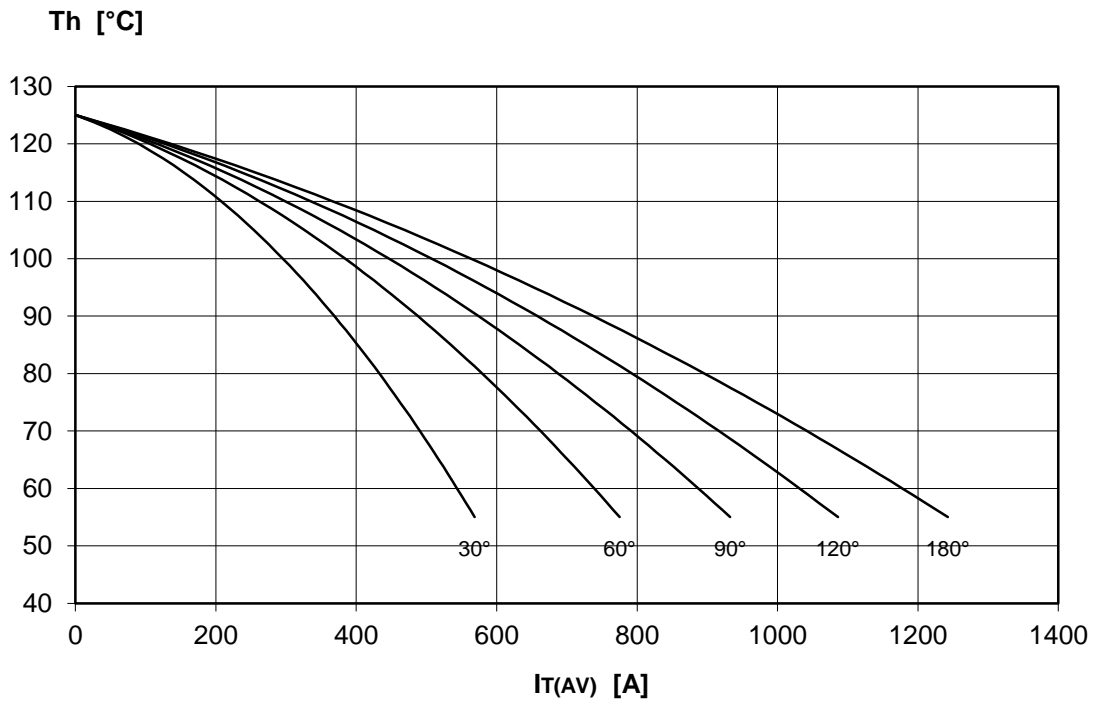
DISSIPATION CHARACTERISTICS

SQUARE WAVE

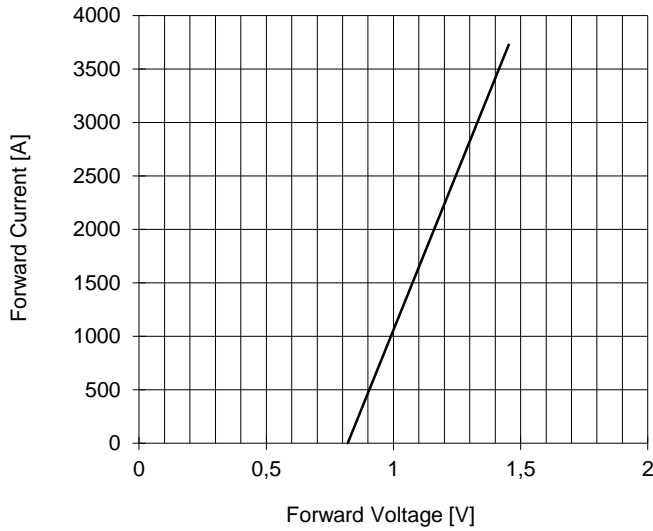


DISSIPATION CHARACTERISTICS

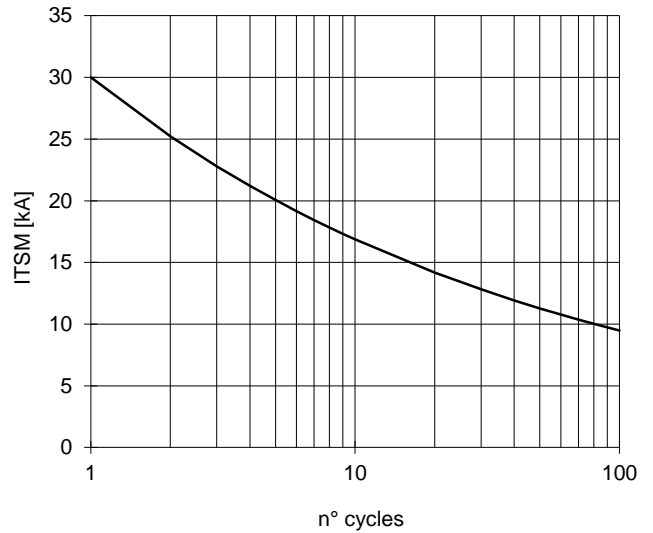
SINE WAVE



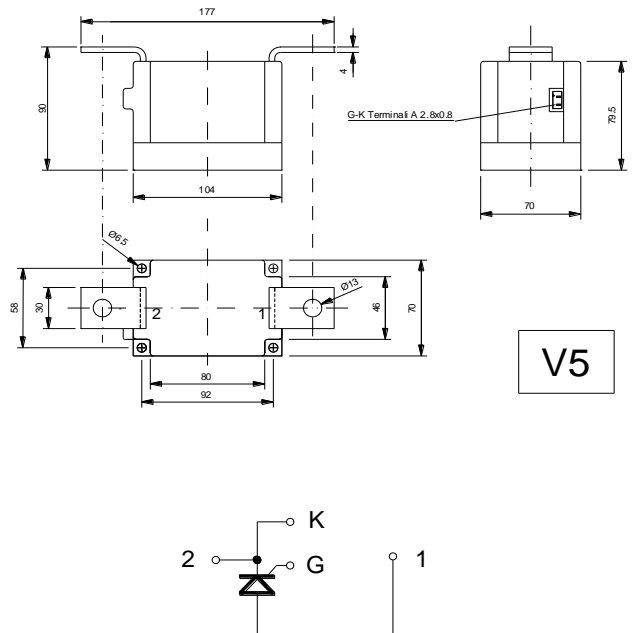
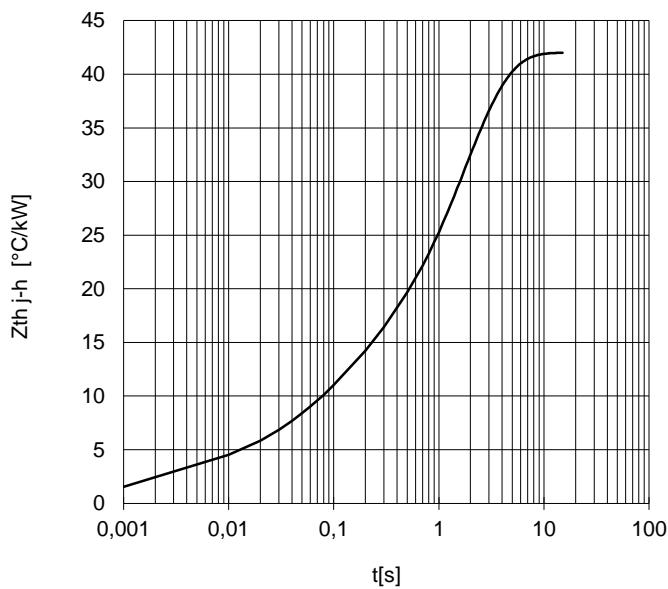
FORWARD CHARACTERISTIC
T_j = 125 °C



SURGE CHARACTERISTIC
T_j = 125 °C



TRANSIENT THERMAL IMPEDANCE
DOUBLE SIDE COOLED



All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < 0.03 mm and roughness < 2 μm. In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice. If not stated otherwise the maximum value of ratings (symbols over shaded background) and characteristics is reported.

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