POSEICO SPA
Via Pillea 42-44, 16153 Genova - ITALY
Tel. + 39 010 8599400 - Fax + 39 010 8682006
Sales Office:
Tel. + 39 010 8599400 - sales@poseico.com

PHASE CONTROL MODULE

ATD571

Repetitive voltage up to **1600 V**
Mean forward current **573 A**
Surge current **14,5 kA**

FINAL SPECIFICATION

apr 17 - ISSUE : 02

Symbol	Characteristic	Conditions	Tj [°C]	Value	Unit
BLOCKING					
V_{RRM}	Repetitive peak reverse/off-state voltage		135	1600	V
V_{RSM}	Non-repetitive peak reverse voltage		135	1700	V
$I_{RRM/DRM}$	Repetitive peak reverse/off-state current		135	50	mA
CONDUCTING					
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Th=91°C, single side cooled		573	A
$I_{T(AV)}$	Mean forward current	180° sin, 50 Hz, Tc=55°C, single side cooled		878	A
I_{TSM}	Surge forward current	Sine wave, 10 ms	135	14,5	kA
I^2t	I^2t	without reverse voltage		1051 x 10^3	A^2s
V_T	On-state voltage	On-state current = 1600 A	25	1,63	V
$V_{T(TO)}$	Threshold voltage		135	1,00	V
r_T	On-state slope resistance		135	0,380	mohm
SWITCHING					
di/dt	Critical rate of rise of on-state current, min.	From 75% VDRM up to 1050 A; gate 10V, 5Ω	135	200	A/µs
dv/dt	Critical rate of rise of off-state voltage, min.	Linear ramp up to 70% of VDRM	135	500	V/µs
t_d	Gate controlled delay time, typical	VD=100V; gate source 25V, 10Ω , tr=.5 µs	25	1,1	µs
t_q	Circuit commutated turn-off time, typical	dv/dt = 20 V/µs linear up to 75% VDRM		200	µs
Q_{rr}	Reverse recovery charge	di/dt = -20 A/µs, I= 700 A	135		µC
I_{rr}	Peak reverse recovery current	VR= 50 V			A
I_H	Holding current, typical	VD=5V, gate open circuit	25	300	mA
I_L	Latching current, typical	VD=5V, tp=30µs	25	700	mA
GATE					
V_{GT}	Gate trigger voltage	VD=5V	25	3,50	V
I_{GT}	Gate trigger current	VD=5V	25	250	mA
V_{GD}	Non-trigger gate voltage, min.	VD=VDRM	135	0,25	V
V_{FGM}	Peak gate voltage (forward)			30	V
I_{FGM}	Peak gate current			10	A
V_{RGM}	Peak gate voltage (reverse)			5	V
P_{GM}	Peak gate power dissipation	Pulse width 100 µs		150	W
P_G	Average gate power dissipation			2	W
MOUNTING					
$R_{th(j-c)}$	Thermal impedance, DC	Junction to case, per element		50,0	°C/kW
$R_{th(c-h)}$	Thermal impedance	Case to heatsink, per element		20,0	°C/kW
T_j	Operating junction temperature			-30 / 135	°C
V_{ins}	RMS insulation voltage	50 hz , circuit to base, all terminal shorted	25	4500	V
T	Mounting torque	Case to heatsink		4 to 6	kN
T	Mounting torque	Busbars to terminal		12 to 18	kN
	Mass			1500	g

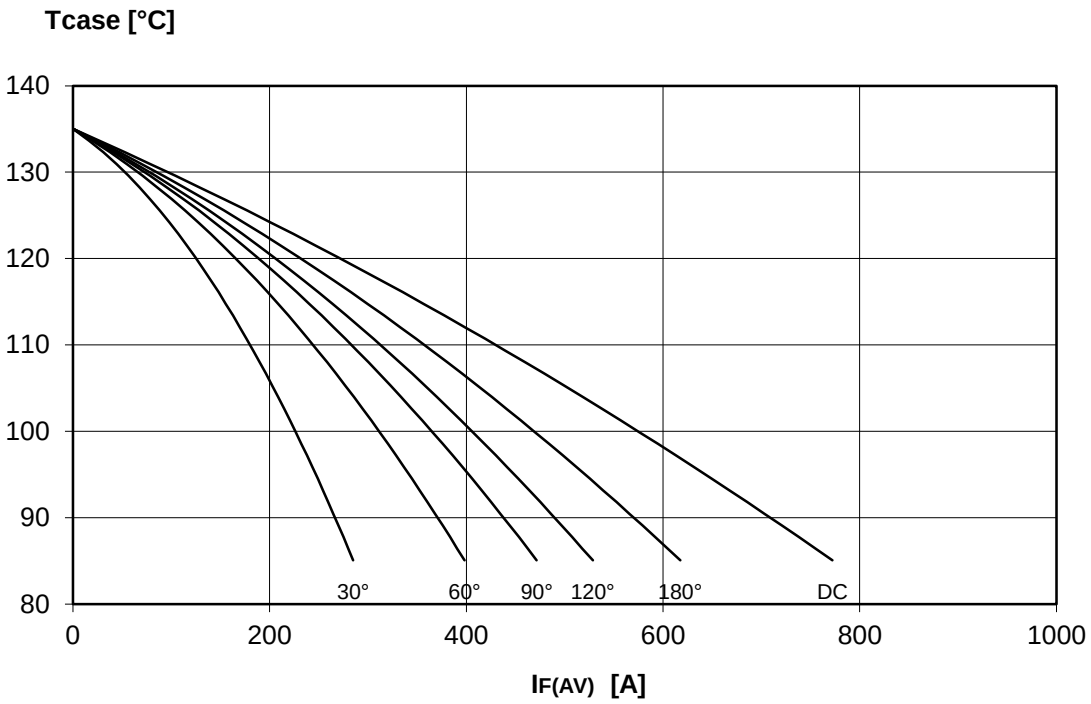
ORDERING INFORMATION : ATD571 S 16

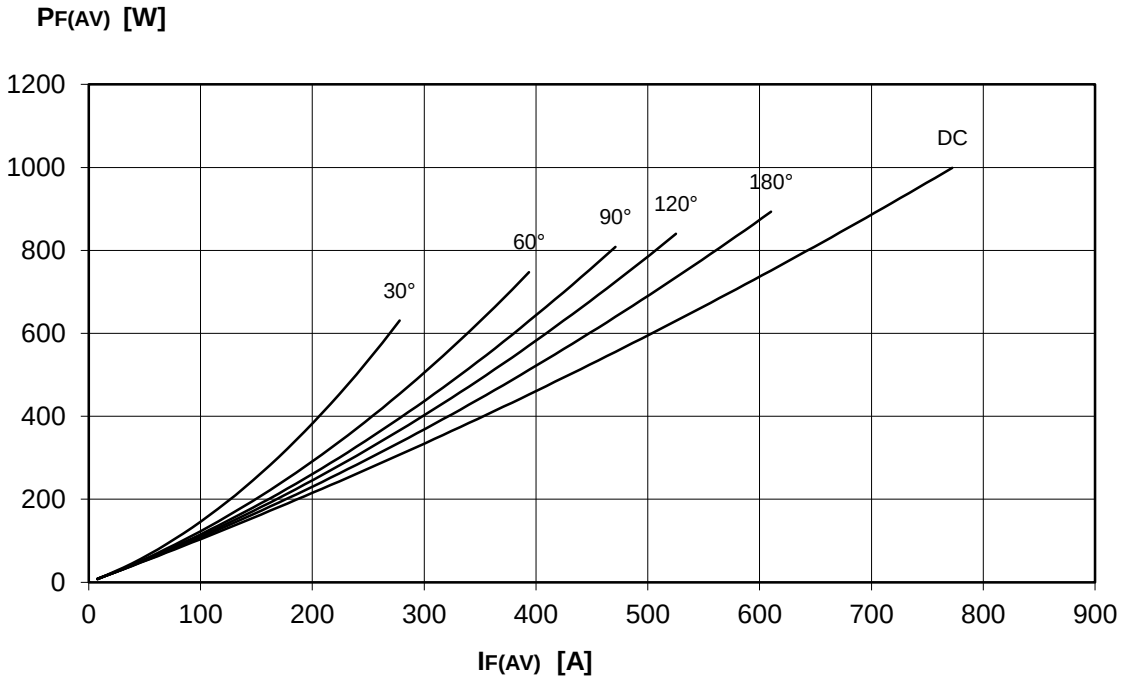
standard specification — VRRM/100

FINAL SPECIFICATION apr 17 - ISSUE : 02

DISSIPATION CHARACTERISTICS

SQUARE WAVE

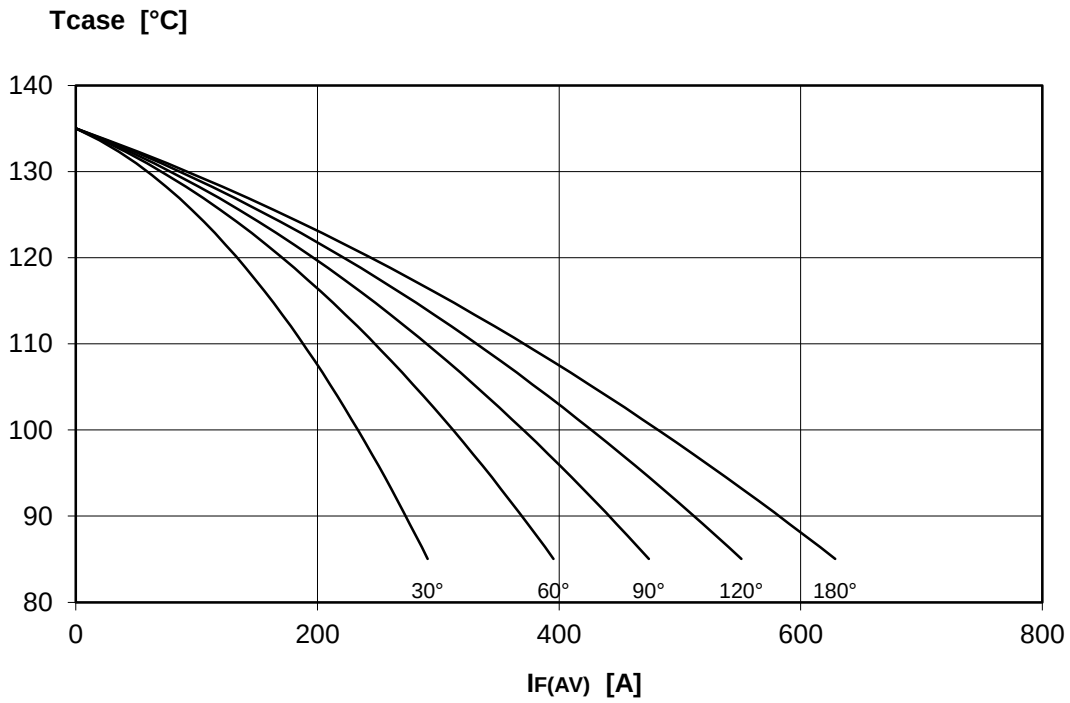


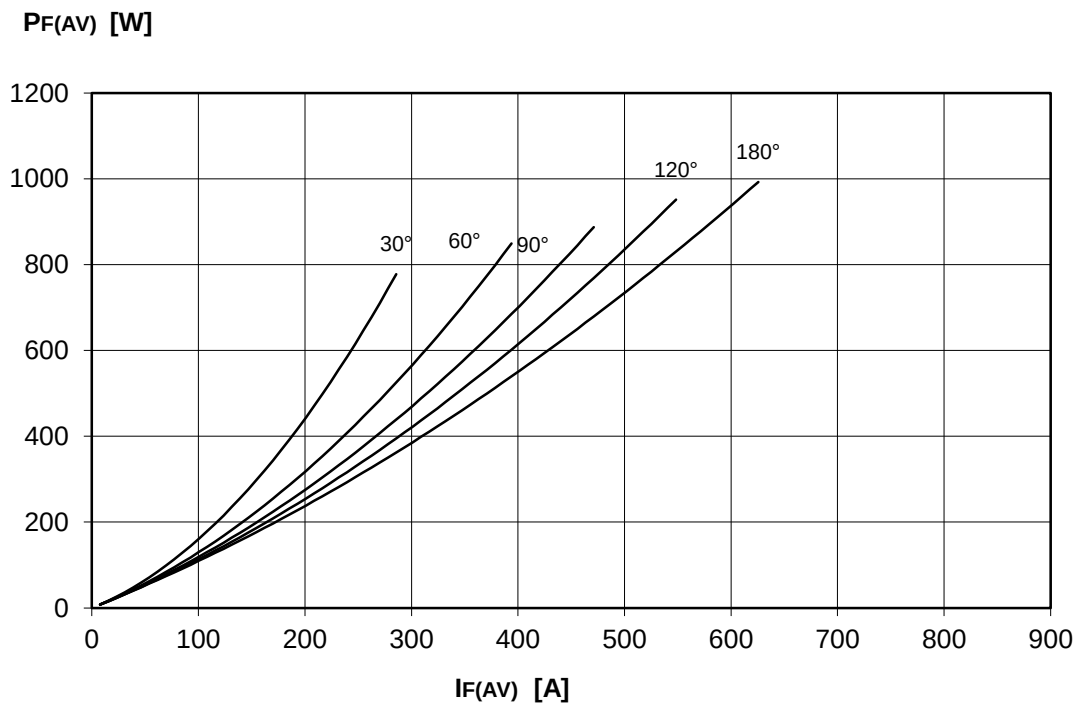


FINAL SPECIFICATION apr 17 - ISSUE : 02

DISSIPATION CHARACTERISTICS

SINE WAVE

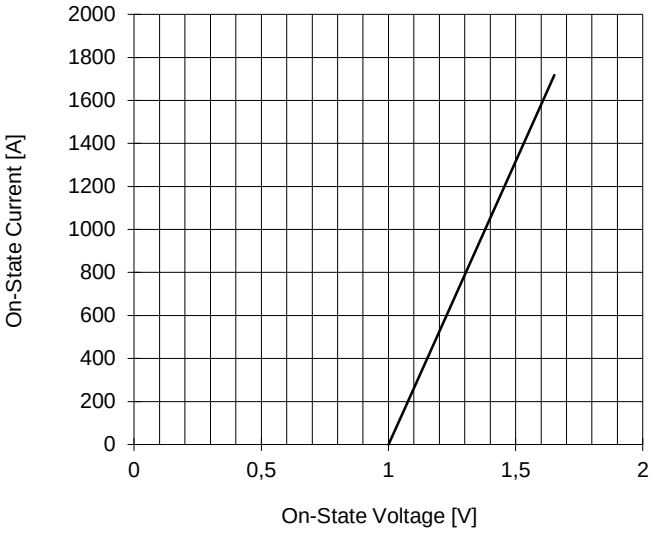




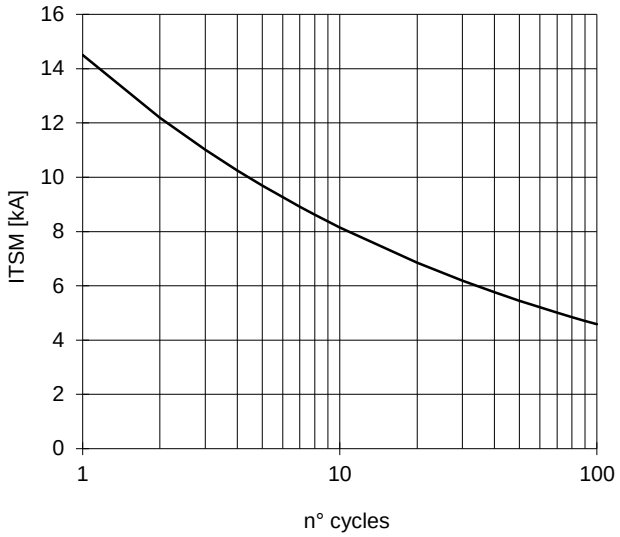
ATD571 PHASE CONTROL MODULE

FINAL SPECIFICATION apr 17 - ISSUE : 02

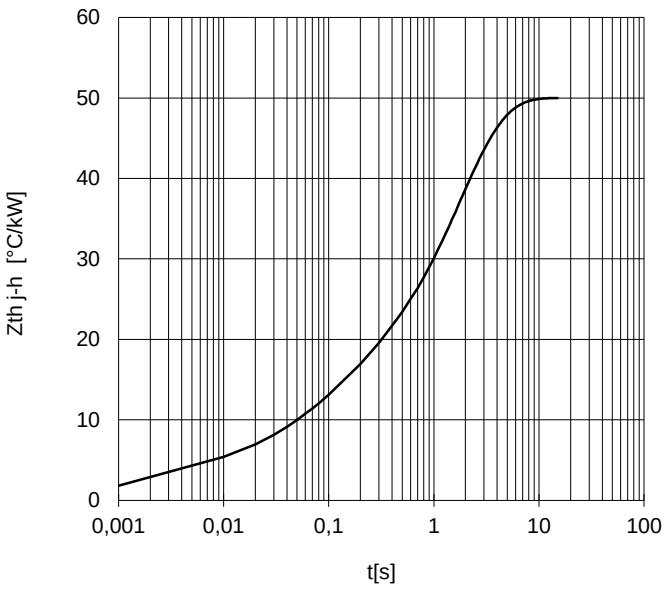
ON-STATE CHARACTERISTIC
Tj = 135 °C

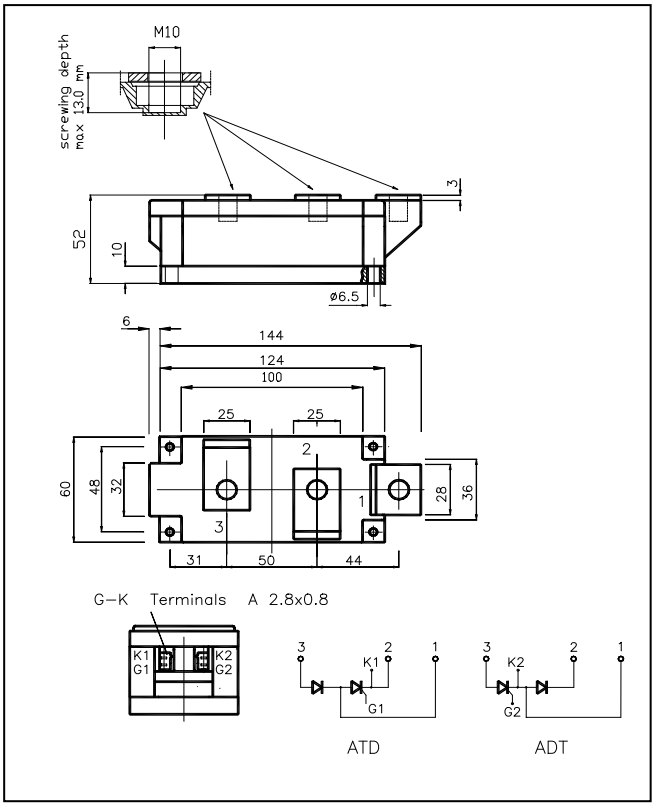


SURGE CHARACTERISTIC
Tj = 135 °C



TRANSIENT THERMAL IMPEDANCE





All the characteristics given in this data sheet are guaranteed only with uniform clamping force, cleaned and lubricated heatsink, surfaces with flatness < .03 mm and roughness < 2 µm.
In the interest of product improvement POSEICO SpA reserves the right to change any data given in this data sheet at any time without previous notice.
If not stated otherwise the maximum value of ratings (simbols over shaded background) and characteristics is reported.

Distributed by